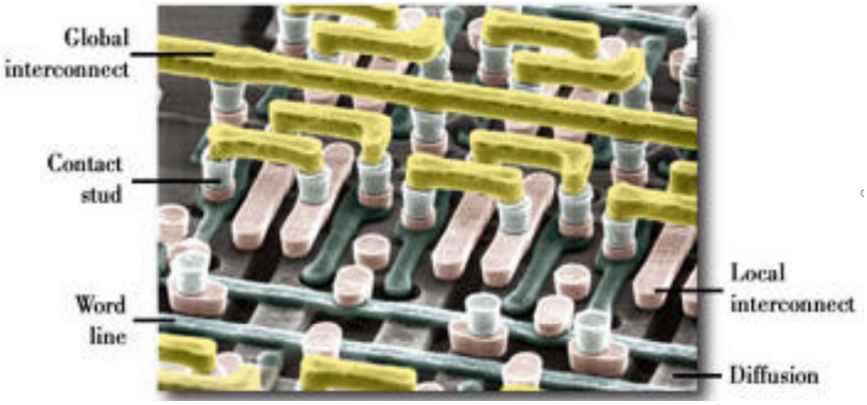
EE 330
Homework Assignment 4
Fall 2022 (Due Friday Sept 16 at 1:00 p.m.)

Problem 1 3.1 of Weste and Harris (WH)

Problem 2 3.2 of WH

Problem 3 If a transistor of length 7nm and width 14nm has a gate oxide thickness of 25A°, how many silicon dioxide molecules will be needed for the gate oxide?

Problem 4 A section of global interconnect (See Fig. 3.12 of WH) is shown below where the SiO_2 insulating material has been removed. If this interconnect were made of aluminum and is 1000μm long, 20nm wide, and 40nm thick, what would be the resistance of the interconnect?



Problem 5 3.5 of WH

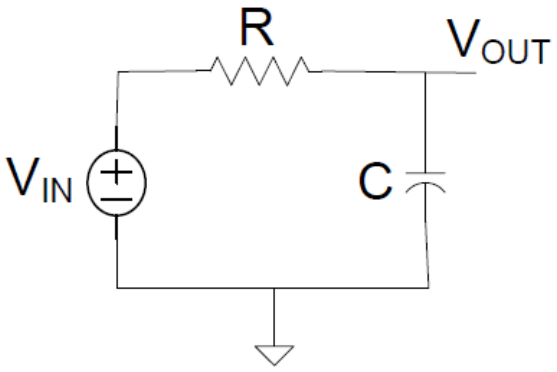
Problem 6 How many 12 inch wafers can be obtained from a 2m silicon pull? Assume the kerf width when a wire saw is used is to cut the wafers is 150μm. In solving this problem, state and use a typical value for the wafer thickness.

Problem 7 A first-order RC filter is shown. The 3-dB band edge of this filter is given by $\omega_{3dB} = \frac{1}{RC}$. Assume Poly 1 with a silicide block is used to make the resistor and the capacitor is a Poly Insulator Substrate capacitor. This filter is to be fabricated in the ON 0.5μ CMOS process that is characterized by the parameters attached to this assignment.

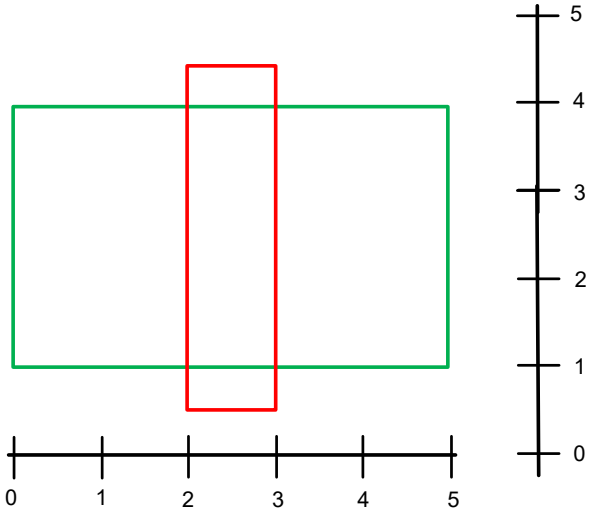
a) Design this circuit and estimate the area required to implement this filter in your design if the 3dB band edge is to be located at 1K Hz and the capacitor value is 8 pF.

b) If the resistor is too big or the capacitor is too big, the area required to realize this filter becomes very large. Determine the value of R and C that will

minimize the total area and compare the area required for the "minimal area" design with that you required in part a). Use a serpentine layout for the resistor.



Problem 8 Consider the layout of a transistor shown below where red is polysilicon and green is n-active. Rulers with dimensions in µm are shown.



a) What is the drawn length and width of the transistor?
b) Assume positive photoresist is used pattern the polysilicon region to protect it during the polysilicon etch. If the photoresist is under-exposed so that the edges move by 0.1µm from the desired location and the photoresist development is perfect, and the polysilicon is under-etched so that the edges move by 0.1µm, what will be the actual length and width of the transistor? (neglect any lateral diffusion that may occur)
c) Repeat part b) if negative photoresist is used.

Problem 9 An aluminum interconnect 250µm long and 2µm wide has a measured resistance of 25Ω. Determine the thickness of the aluminum interconnect and the sheet resistance. If a copper interconnect has the same thickness and the same width as the aluminum interconnect, how long would it be if it also had the same resistance?

Problem 10 Thermal oxide growth of field oxide causes the wafer surface to become somewhat nonplanar. If 5000Å of field oxide is thermally grown, what is the difference in the thickness of the wafer between regions where field oxide is present and where it is absent. In solving this problem, state and use a typical value for the wafer thickness.

Measured Parameters for an ON 0.5µm CMOS Process

MINIMUM	3.0/0.6			
Vth		0.78	-0.93	volts
SHORT	20.0/0.6			
Idss		439	-238	uA/um
Vth		0.69	-0.90	volts
Vpt		10.0	-10.0	volts
WIDE	20.0/0.6			
Ids0		< 2.5	< 2.5	pA/um
LARGE	50/50			
Vth		0.70	-0.95	volts
Vjbkd		11.4	-11.7	volts
Ijlk		<50.0	<50.0	pA
Gamma		0.50	0.58	V^0.5
K' (Uo*Cox/2)		56.9	-18.4	uA/V^2
Low-field Mobility		474.57	153.46	cm^2/V*s

COMMENTS: XL_AMI_C5F

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>15.0	<-15.0	volts

PROCESS PARAMETERS	N+ACTV	P+ACTV	POLY	PLY2_HR	POLY2	MTL1	MTL2	UNITS
Sheet Resistance	82.7	103.2	21.7	984	39.7	0.09	0.09	ohms/sq
Contact Resistance	56.2	118.4	14.6		24.0		0.78	ohms
Gate Oxide Thickness	144							angstrom

PROCESS PARAMETERS	MTL3	N\PLY	N_WELL	UNITS
Sheet Resistance	0.05	824	815	ohms/sq
Contact Resistance	0.78			ohms

COMMENTS: N\POLY is N-well under polysilicon.

CAPACITANCE PARAMETERS	N+ACTV	P+ACTV	POLY	POLY2	M1	M2	M3	N_WELL	UNITS
Area (substrate)	429	721	82		32	17	10	40	aF/um^2
Area (N+active)			2401		36	16	12		aF/um^2
Area (P+active)			2308						aF/um^2
Area (poly)				864	61	17	9		aF/um^2
Area (poly2)					53				aF/um^2
Area (metal1)						34	13		aF/um^2
Area (metal2)							32		aF/um^2
Fringe (substrate)	311	256			74	58	39		aF/um
Fringe (poly)					53	40	28		aF/um
Fringe (metal1)						55	32		aF/um
Fringe (metal2)							48		aF/um
Overlap (N+active)			206						aF/um
Overlap (P+active)			278						aF/um